REMARKS/ARGUMENT

Claims 9-22 are now presented for examination. Claims 9-11 and 13-20 have been amended. Claim 22 has been added to provide Applicant with a more complete scope of protection.

Claims 9 and 20 are the only independent claims.

Claims 9-15 (and apparently 19-21) were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent 5,396,098 (Kim et al.). Claims 16-18 were rejected under 35 U.S.C. § 103 as obvious from Kim et al. in view of U.S. Patent 5,595,922 (Tigelaar et al.). Applicant submits that independent claims 9 and 20 are patentable over the cited prior art for at least the following reasons.

Claim 9 is directed to a method of manufacturing a semiconductor device comprising at least first and second MOS transistors. The method comprises: providing a semiconductor substrate having at least first and second active regions of a first conductivity type and at least third and fourth active regions of a second conductivity type opposite to the first conductivity type; forming a gate oxide layer having a first thickness onto at least the first, second, third and fourth active regions; forming an electrode layer of non-doped polysilicon onto the gate oxide layer; patterning the electrode layer to form first, second, third and fourth gate electrodes onto the first, second, third and fourth active regions, respectively; doping the first active region and the first gate electrode with an impurity of the second conductivity type to form a first transistor driven at a first voltage level, the first gate electrode being doped at a first concentration; doping the second active region and the second gate electrode with an impurity of the second conductivity type to form a second transistor to be driven at a second voltage level lower than the first voltage level, the second gate electrode being doped at a second concentration higher than the first concentration; doping the third active region and the third gate electrode with an impurity of the first conductivity type to form a third

transistor to be driven at the first voltage level, the third gate electrode being doped at a third concentration; and doping the fourth active region and the fourth gate electrode with an impurity of the first conductivity type to form a fourth transistor to be driven at the second voltage level, the fourth gate electrode being doped at a fourth concentration higher than the third concentration. The recited structure includes high and low voltage n-channel transistors and high and low voltage p-channel transistors.

Kim et al. shows an NAND type ROM. However, Applicant fails to find in Kim et al. any teaching or suggestion of the features of amended claim 1 recited above. For at least that reason, amended claim 1 is believed clearly patentable over Kim et al.

Claim 20 is directed to a method of manufacturing a semiconductor device. The method comprises: (a) doping a high voltage CMOS circuit at a low impurity concentration; and (b) doping a low voltage CMOS circuit at a high impurity concentration after the step (a). Claim 21, further comprises: (c) forming a sidewall spacer after the step (a) and before the step (b).

Kim et al., shows how to manufacture a NAND type ROM, but contains no teaching or suggestion of how to make multi-voltage CMOS transistors, as in the present invention. For at least this reason, amended independent claim 20 is believed patentable over Kim et al.

The other claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual consideration or reconsideration, as the case may be, of the patentability of each on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

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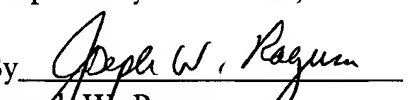
Respectfully submitted,

By 

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